



# Improved Current Mode PWM Controller

## FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

## DESCRIPTION

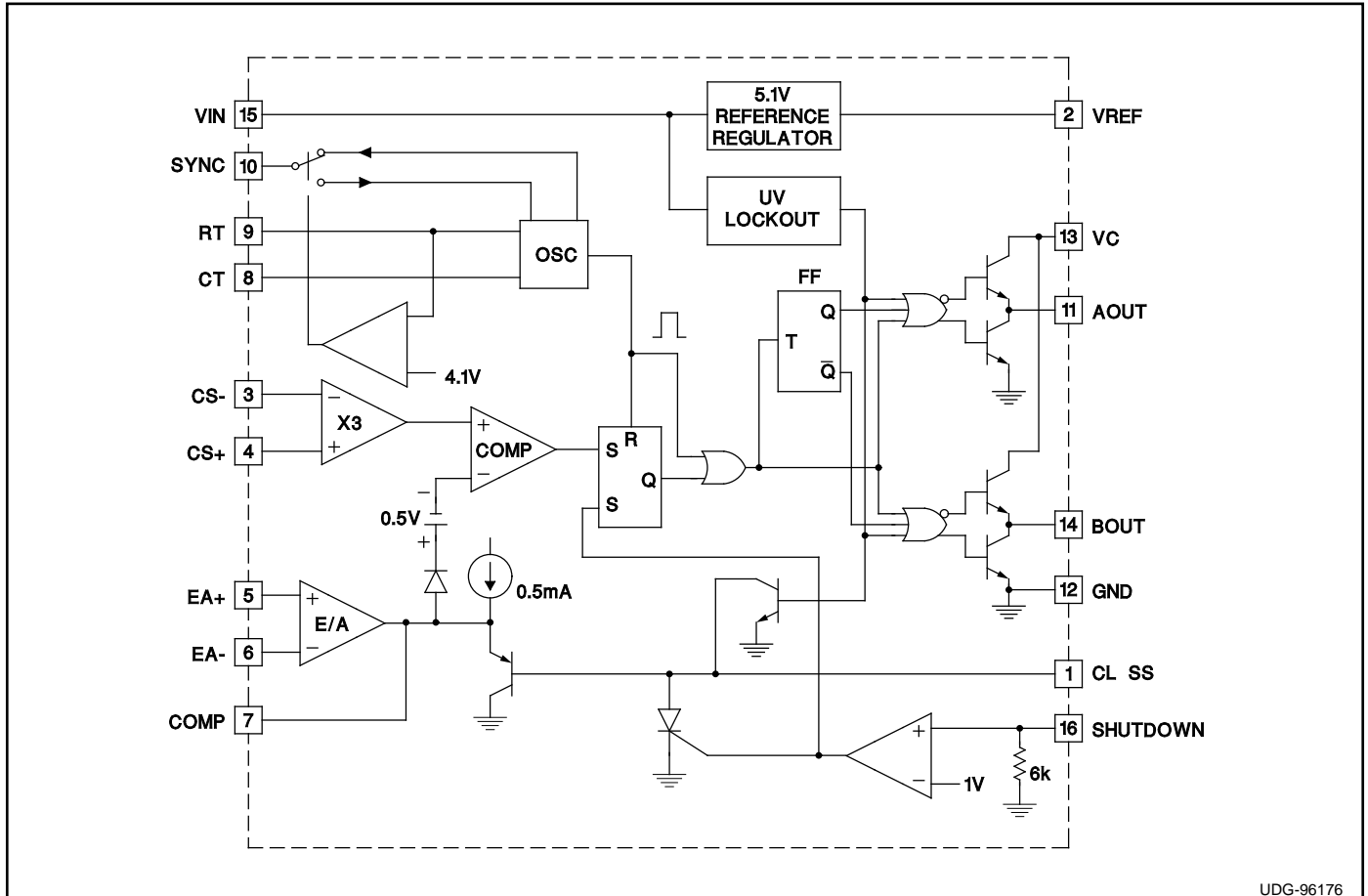
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

## BLOCK DIAGRAM



UDG-96176

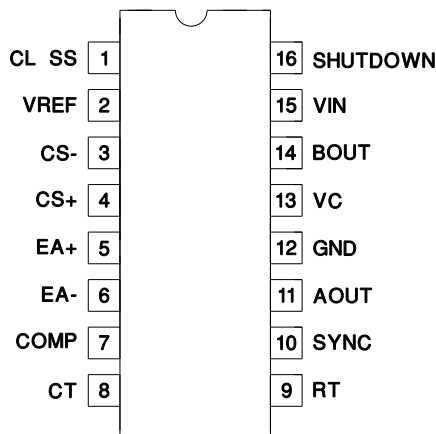
### ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	+40V
Collector Supply Voltage .....	+40V
Output Current, Source or Sink	
DC .....	0.5A
Pulse (0.5 $\mu$ s) .....	2.0A
Error Amp Inputs .....	-0.3V to +VIN
Shutdown Input .....	-0.3V to +10V
Current Sense Inputs .....	-0.3V to +3V
SYNC Output Current .....	$\pm$ 10mA
Error Amplifier Output Current .....	-5mA
Soft Start Sink Current .....	50mA
Oscillator Charging Current .....	5mA
Power Dissipation at TA = 25°C (Note 2) .....	1000mW
Power Dissipation at TC = 25°C (Note 2) .....	2000mW
Junction Temperature .....	-55°C to +150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....	+300°C

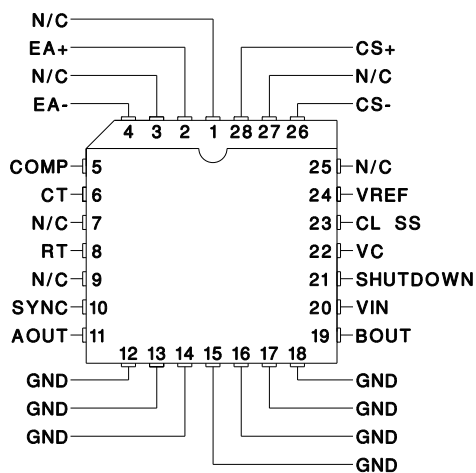
All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

### CONNECTION DIAGRAMS

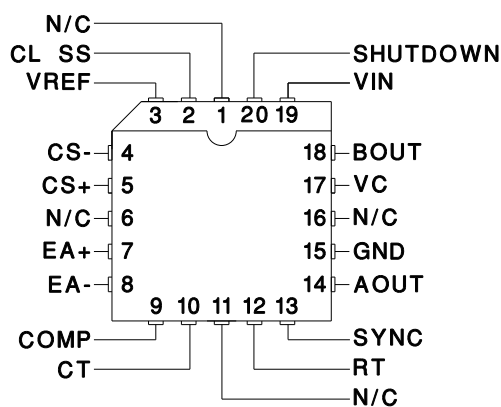
DIL-16, SOIC-16 (Top View)  
J or N, DW PACKAGE



PLCC-28 (Top View)  
QP PACKAGE



PLCC-20 (Top View)  
Q PACKAGE



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for UC1856; -40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	VIN = 8V to 40V			20			20	mV
Load Regulation	Io = -1mA to -10mA			15			15	mV
Total Output Variation	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz < f < 10kHz, TJ = 25°C		50			50		$\mu$ V
Long Term Stability	TJ = 125°C, 1000 Hrs (Note 2)		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-25	-45	-65	-25	-45	-65	mA
<b>Oscillator Section</b>								
Initial Accuracy	TJ = 25°C	180	200	220	180	200	220	kHz
	Over Operating Range	170		230	170		230	kHz

**ELECTRICAL CHARACTERISTICS (cont.)** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for UC1856;  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2856; and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3856,  $V_{IN} = 15\text{V}$ ,  $R_T = 10\text{k}$ ,  $C_T = 1\text{nF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Oscillator Section (cont.)</b>								
Voltage Stability	$V_{IN} = 8\text{V to }40\text{V}$			2			2	%
Discharge Current	$T_J = 25^\circ\text{C}$ , $V_{CT} = 2\text{V}$	7.5	8.0	8.8	7.5	8.0	8.8	mA
	$V_{CT} = 2\text{V}$	6.7	8.0	8.8	6.7	8.0	8.8	mA
Sync Output High Level	$I_o = -1\text{mA}$	2.4	3.6		2.4	3.6		V
Sync Output Low Level	$I_o = +1\text{mA}$		0.2	0.4		0.2	0.4	V
Sync Input High Level	$C_T = 0\text{V}$ , $R_T = V_{REF}$	2.0	1.5		2.0	1.5		V
Sync Input Low Level	$C_T = 0\text{V}$ , $R_T = V_{REF}$		1.5	0.8		1.5	0.8	V
Sync Input Current	$C_T = 0\text{V}$ , $R_T = V_{REF}$ $V_{SYNC} = 5\text{V}$		1	10		1	10	$\mu\text{A}$
Sync Delay to Outputs	$C_T = 0\text{V}$ , $R_T = V_{REF}$ $V_{SYNC} = 0.8\text{V to }2\text{V}$		50	100		50	100	ns
<b>Error Amplifier Section</b>								
Input Offset Voltage	$V_{CM} = 2\text{V}$			5			10	mV
Input Bias Current				-1			-1	$\mu\text{A}$
Input Offset Current				500			500	nA
Common Mode Range	$V_{IN} = 8\text{V to }40\text{V}$	0		$V_{IN} - 2$	0		$V_{IN} - 2$	V
Open Loop Gain	$V_o = 1.2\text{V to }3\text{V}$	80	100		80	100		dB
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$	1	1.5		1	1.5		MHz
CMRR	$V_{CM} = 0\text{V to }38\text{V}$ , $V_{IN} = 40\text{V}$	75	100		75	100		dB
PSRR	$V_{IN} = 8\text{V to }40\text{V}$	80	100		80	100		dB
Output Sink Current	$V_{ID} = -15\text{mV}$ , $V_{COMP} = 1.2\text{V}$	5	10		5	10		mA
Output Source Current	$V_{ID} = 15\text{mV}$ , $V_{COMP} = 2.5\text{V}$	-0.4	-0.5		-0.4	-0.5		mA
Output High Level	$V_{ID} = 50\text{mV}$ , $R_L (\text{COMP}) = 15\text{k}$	4.3	4.6	4.9	4.3	4.6	4.9	V
Output Low Level	$V_{ID} = -50\text{mV}$ , $R_L (\text{COMP}) = 15\text{k}$		0.7	1		0.7	1	V
<b>Current Sense Amplifier Section</b>								
Amplifier Gain	$V_{CS-} = 0\text{V}$ , CL SS Open (Notes 3,4)	2.5	2.75	3.0	2.5	2.75	3.0	V/V
Maximum Differential Input Signal ( $V_{CS+} - V_{CS-}$ )	CL SS Open (Note 3) $R_L (\text{COMP}) = 15\text{k}$	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{CL\text{ ss}} = 0.5\text{V}$ COMP Open (Note 3)		5	35		5	35	mV
CMRR	$V_{CM} = 0\text{V to }3\text{V}$	60			60			dB
PSRR	$V_{IN} = 8\text{V to }40\text{V}$	60			60			dB
Input Bias Current	$V_{CL\text{ ss}} = 0.5\text{V}$ , COMP Open (Note 3)			-1	-3	-1	-3	$\mu\text{A}$
Input Offset Current	$V_{CL\text{ ss}} = 0.5\text{V}$ , COMP Open (Note 3)			1			1	mA
Input Common Mode Range		0		3	0		3	V
Delay to Outputs	$V_{EA+} = V_{REF}$ , $E_{A-} = 0\text{V}$ $CS+ - CS- = 0\text{V to }1.5\text{V}$		120	250		120	250	ns
<b>Current Limit Adjust Section</b>								
Current Limit Offset	$V_{CS-} = 0\text{V}$ $V_{CS+} = 0\text{V}$ , COMP = Open (Note 3)	0.43	0.5	0.57	0.43	0.5	0.57	V
Input Bias Current	$V_{EA+} = V_{REF}$ , $V_{EA-} = 0\text{V}$		-10	-30		-10	-30	$\mu\text{A}$
<b>Shutdown Terminal Section</b>								
Threshold Voltage		0.95	1.00	1.05	0.95	1.00	1.05	V
Input Voltage Range		0		5	0		5	V

**ELECTRICAL CHARACTERISTICS (cont.)** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for UC1856;  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2856; and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3856,  $V_{IN} = 15\text{V}$ ,  $R_T = 10\text{k}$ ,  $C_T = 1\text{nF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Shutdown Terminal Section (cont.)</b>								
Minimum Latching Current (I <sub>CL SS</sub> )	(Note 5)	3	1.5		3	1.5		mA
Maximum Non-Latching Current (I <sub>CL SS</sub> )	(Note 6)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	V <sub>SHUTDOWN</sub> = 0 to 1.3V		65	110		65	110	ns
<b>Output Section</b>								
Collector-Emitter Voltage		40			40			V
Off-State Bias Current	V <sub>C</sub> = 40V			250			250	μA
Output Low Level	I <sub>OUT</sub> = 20mA		0.1	0.5		0.1	0.5	V
	I <sub>OUT</sub> = 200mA		0.5	2.6		0.5	2.6	V
Output High Level	I <sub>OUT</sub> = -20mA	12.5	13.2		12.5	13.2		V
	I <sub>OUT</sub> = -200mA	12	13.1		12	13.1		V
Rise Time	C <sub>1</sub> = 1nF		40	80		40	80	ns
Fall Time	C <sub>1</sub> = 1nF		40	80		40	80	ns
UVLO Low Saturation	V <sub>IN</sub> = 0V, I <sub>OUT</sub> = 20mA		0.8	1.5		0.8	1.5	V
<b>PWM Section</b>								
Maximum Duty Cycle		45	47	50	45	47	50	%
Minimum Duty Cycle				0			0	%
<b>Undervoltage Lockout Section</b>								
Startup Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.7			0.7		V
<b>Total Standby Current</b>								
Supply Current			18	23		18	23	mA

Note 1: All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

Note 2: This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.

Note 3: Parameter measured at trip point of latch with  $V_{EA+} = V_{REF}$ ,  $V_{EA-} = 0\text{V}$ .

Note 4: Amplifier gain defined as:

$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}; \quad \Delta V_{CS-} = 0\text{V to } 1.0\text{V}$$

Note 5: Current into CL SS guaranteed to latch circuit into shutdown state.

Note 6: Current into CL SS guaranteed not to latch circuit into shutdown state.

APPLICATIONS INFORMATION

### Oscillator Circuit

Output deadtime is determined by size of the external capacitor,  $C_T$ , according to the formula:  $T_d = \frac{2C_T}{8mA - \frac{3.6}{RT}}$

For large values of  $R_T$ :  $T_d = 250C_T$

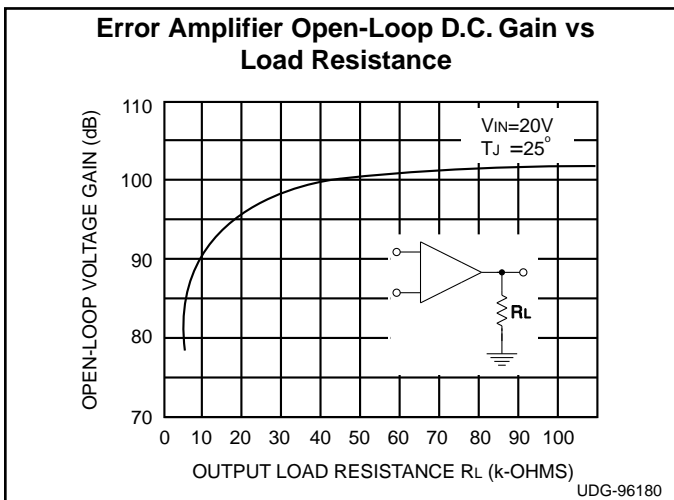
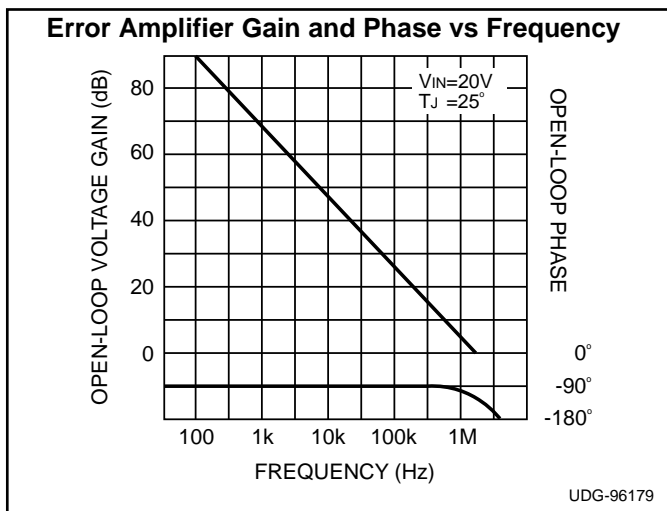
Oscillator frequency is approximated by the formula:  $f_T = \frac{2}{R_T C_T}$

UDG-96177

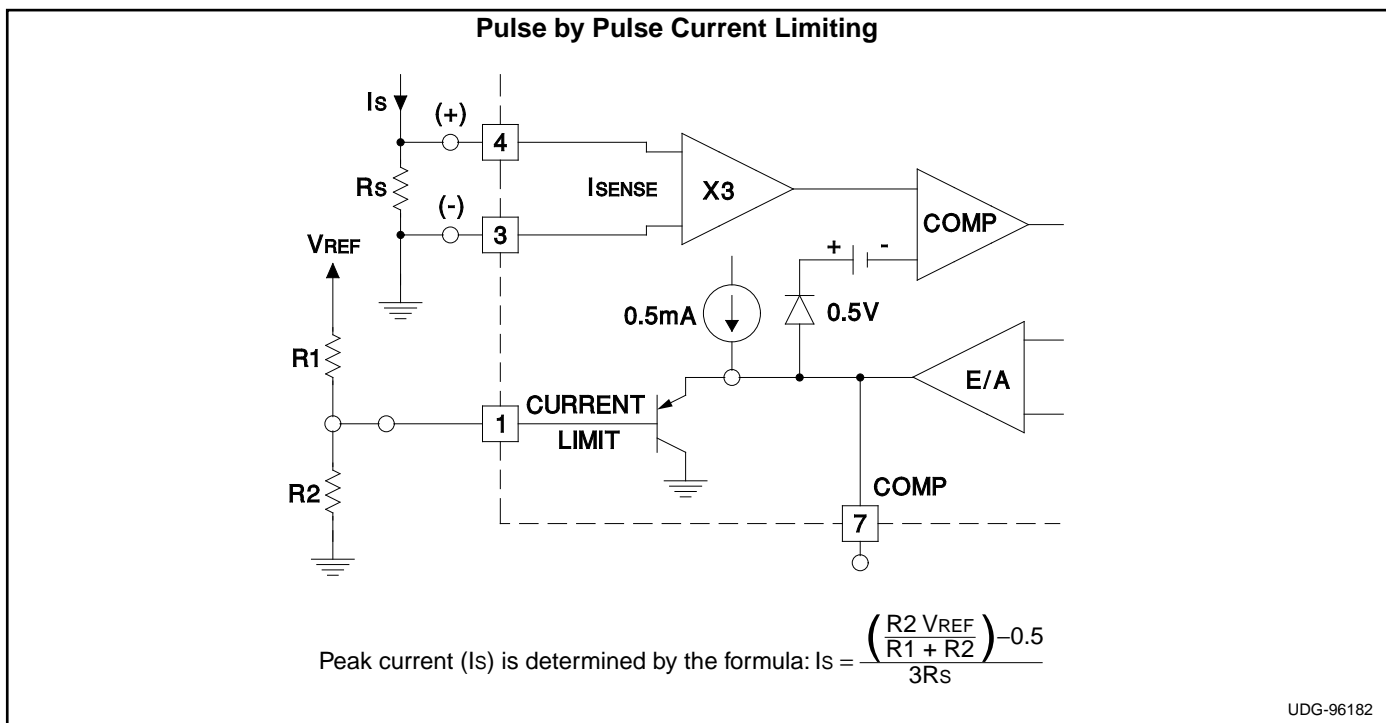
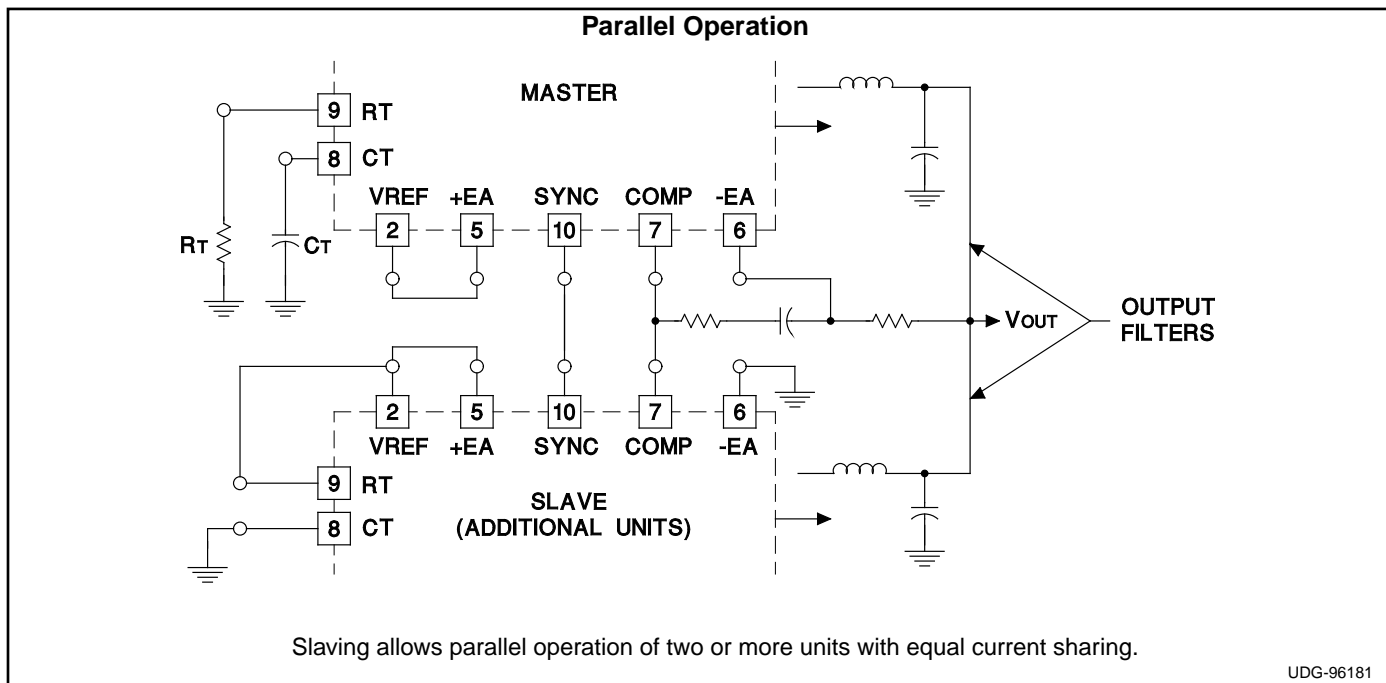
### Error Amplifier Output Configuration

Error Amplifier can source up to 0.5mA.

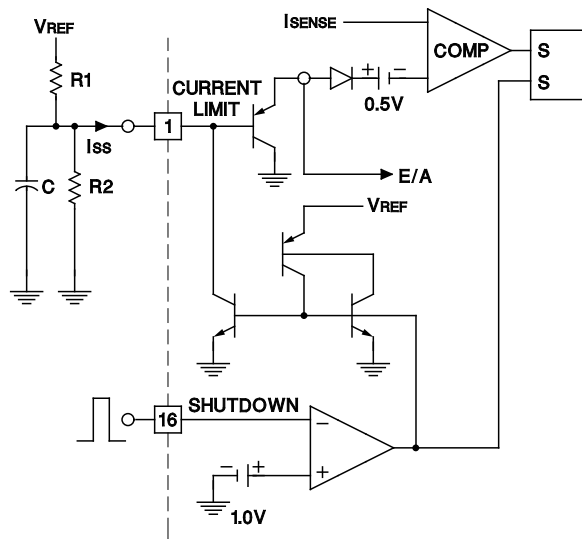
UDG-96178



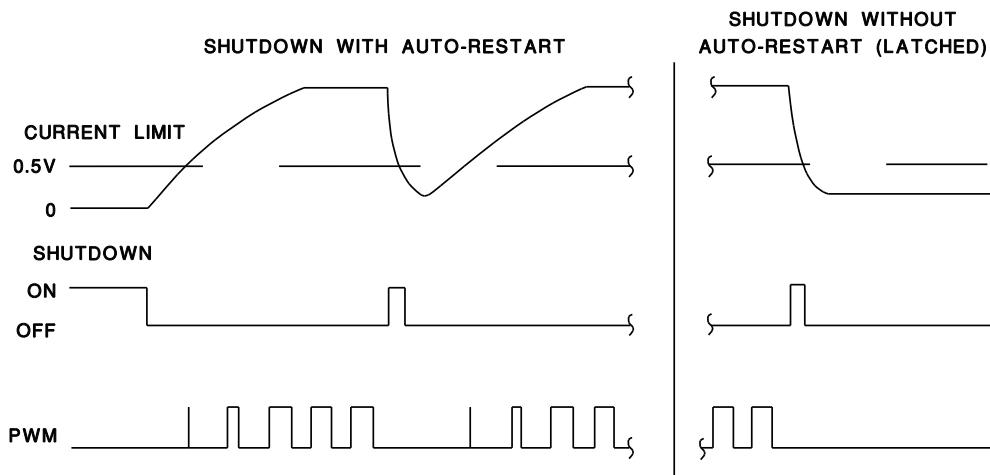
APPLICATIONS INFORMATION (cont.)



APPLICATIONS DATA (cont.)



UDG-96183

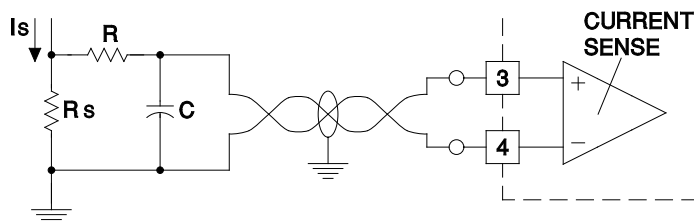


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If  $\frac{V_{REF}}{R1} < 0.8\text{mA}$ , the shutdown latch will commutate when  $I_{ss} = 0.8\text{mA}$  and a restart cycle will be initiated.

If  $\frac{V_{REF}}{R1} < 3\text{mA}$ , the device will latch off until power is recycled.

Current Sense Amplifier Connections



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise sensing.

UDG-96185

APPLICATIONS INFORMATION (cont.)

